Remarks

Claims 1-16 remain pending in this application. The undersigned thanks the Examiner and his Supervisor for taking the time to conduct the telephone interview regarding this proposed Amendment on this same date. As discussed during the interview, Claims 1, 5, 9 and 13 have been amended in accordance with the Examiner's remarks set forth in the "Response to Arguments" section of the Office Action for overcoming the present claim rejections under 35 U.S.C. Section 103 over the Kagawa reference combined with the Nishiuma reference.

Regarding independent method of manufacture claims 1 and 5, the order of the steps now require that the transistor die be secured to the device substrate prior to measurement of a performance characteristic, and that the impedance of the one or more wires be set after the performance characteristic is measured. Method claims 2-4 and 6-8 depend from respective claims 1 and 5, and are now believed to be in allowable form for this same reason.

Regarding the "product by process" independent claims 9 and 13, each clearly requires that the impedance of the one or more wires is selected based at least in part on a performance characteristic of the transistor measured after the die is secured to the substrate. Claims 10-12 and 14-16 depend respective claims 9 and 13, and are now believed to be in allowable form for this same reason.

Conclusion

A marked-up version of the amended claims is attached hereto. In view of the amendment being to put the claims in allowable form as recognized by the Examiner, entry of this Amendment and allowance of the application is respectfully requested. If the Examiner has any questions regarding this paper or the application in general, he is invited to call the undersigned at the number listed below.

Respectfully submitted,

Bingham McCutchen LLP

Dated: 10-3-02

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Enclosure: Marked up version of the amended claims pursuant to 37 C.F.R. § 1.121(c)(1)(ii).

Marked-up version of the amended claims, showing the changes:

1. (Amended) A method of manufacturing a power transistor circuit, comprising carrying out the following steps in the enumerated order:

(1) securing a die to a substrate, the die comprising a transistor having an input terminal;

(2) measuring a performance characteristic of the transistor;

(3) using one or more wires to electrically couple the transistor input terminal to an input matching element, an input signal lead, or both; and

(4) setting the impedance of the one or more wires based at least in part on the measured transistor performance characteristic from step (2).

5. (Amended) A method of manufacturing a power transistor circuit, comprising carrying out the following steps in the enumerated order:

(1) securing a die to a substrate, the die comprising a transistor having an output terminal;

(2) measuring a performance characteristic of the transistor;

(3) using one or more wires to electrically couple the transistor output terminal to an output matching element, an output signal lead, or both; and

(4) setting the impedance of the one or more wires based at least in part on the measured transistor performance characteristic from step (2).

9. (Amended) A power transistor circuit, comprising:

a substrate;

a die secured to the substrate, the die comprising a transistor having an input terminal;

one or both of an input lead and an input matching element secured to the substrate; and

one or more wires electrically coupling the transistor input terminal to the one or both of the input matching element and input signal lead, wherein the impedance of the one or more wires is selected based at least in part on a performance characteristic of the transistor measured after the die is secured to the substrate.

13. (Amended) A power transistor circuit, comprising:

a substrate;

a die secured to the substrate, the die comprising a transistor having an output terminal;

one or both of an output lead and an output matching element secured to the substrate; and

one or more wires electrically coupling the transistor output terminal to the one or both of the output matching element and output signal lead, wherein the impedance of the one or more wires is selected based at least in part on a performance characteristic of the transistor measured after the die is secured to the substrate.